

GOWINSEMI's Arora V FPGA series provides SRAM-based FPGA devices with increased logic resources, interfaces and performance. Arora V FPGAs include DDR3 memory interfacing, 12.5Gbps CDR-based SERDES supporting multiple protocols and flexible packaging options making it the ideal choice for communications, server, imaging, and automotive applications requiring high interface and computing throughput by providing best performance/watt.

Arora V Features

Arora V is supported by GOWIN EDA providing an efficient and easy-to-use FPGA hardware development environment support multiple RTL-based programming languages, synthesis, placement & routing, bitstream generation and download, power analysis and in-device logic analyser.

Ultra-Efficient Low Power

- * Advanced 22m LP process
- * Low Core Voltage - 1.0V & 0.9V
- * Dynamic Clock Gating

Multichannel High Speed SERDES

- * 8x Transceivers 270Mbps to 12.5Gbps.
- SERDES custom protocols including 10Gb Ethernet

Hardcore PCIe2.1

- * Supports x1, x2, x4, x8 Endpoints and Root Port
- * Including Root Complex and End Point Dual-Mode

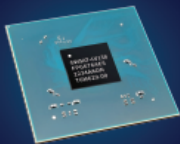
Hardcore MIPI D-PHY

- * MIPI DSI-2 and CSI-2 device interfaces
- * MIPI Data-Rate 2.5Gbps/lane
- * MIPI bandwidth 20Gbps with up to 8 Data-Lanes and Clock-Lanes

- DDR Rate 1333Mbps
- Integrated ADC supports On-Chip Temperature Measurement
- Single Event Upset (SEU) Mitigation
- Programming Support

- * JTAG, SSPI, MSPI, CPU, and SERIAL Modes Background programming, SPI Flash Programming and Boot, Multi-boot

Arora[®]-V Product Features



High-Speed DPHY

GPIO supports DPHY TX/RX up to 2.5Gbps

CPHY

GPIO supports CPHY RX/TX up to 2.5Gbps

Radiation Resistance

Proprietary ECC and advanced SRAM design for better SER mitigation

High Performance & Flexible DPHY Hard Core

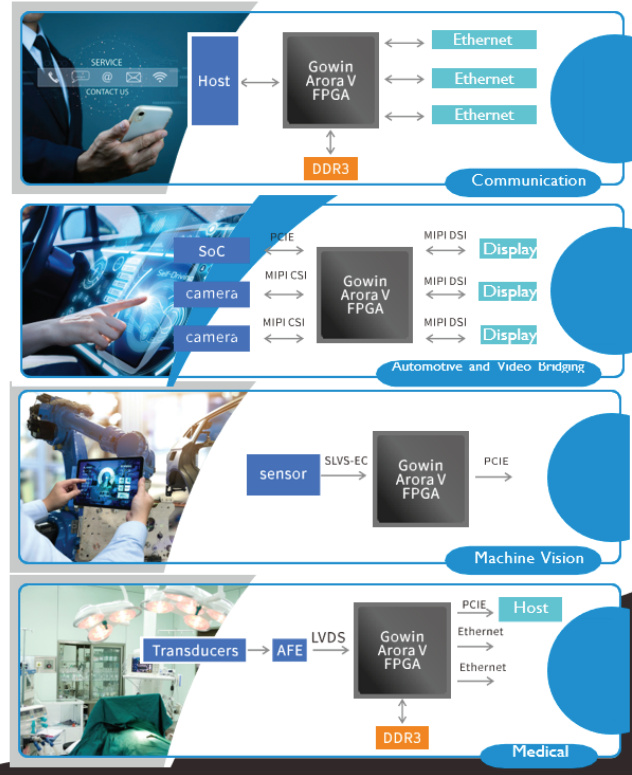
Hardcore DPHY TX/RX up to 3Gbps; A Flexible PHY can support two lane inputs, two lane outputs.

GPIO supports CDR

GPIO can support CDR with bit rate up to 2.5Gbps; Covering Serdes low speed operation for lower power consumption. Supports USB2.0 HS, SGMII 1.25Gbps, PON 1.25Gbps or low speed DP, HDMI, LVDS7:1 and so on.

Device	GW5A(R)T-15	GW5A(R/S)-25	GW5A(R/S)T-60	GW5A(R)T-75	GW5A(S/R)T-138
Logic Unit (LUT4)	15,120	23,040	59,904	86,688	138,240
Register (REG)	15,120	23,040	59,904	86,688	138,240
SSRAM(Kbits)	118	180	468	677	1,080
BSRAM(Kbits)	630	1,008	2,070	6,120	6,120
BSRAM(unit)	35	56	115	256	340
DSP (27x18 or two 12x12)	34	28	117	213	298
PLL(1)	2	6	8	12	12
Global Clock	16	16	16	16	16
High Speed Clock	8	16	20	24	24
Transceivers	4	0	4	8	8
Transceivers bit rate	270Mbps-10Gbps	-	270Mbps-12.5Gbps	-	270Mbps-12.5Gbps
PCIe 2.0 Hard Core	1,x1,x2,x4 PCIe 2.0	0	1,x1,x2,x4 PCIe 2.0	1,x1,x2,x4 PCIe 2.0	1,x1,x2,x4,x8 PCIe 2.0
LVDS (Gbps)	1.25	1.25	1.25	1.25	1.25
DDR3 (Mbps)	1066	1066	1,333	1,333	1,333
MIPI D-PHY Hard Core	2.5Gbps (RX/TX) 4 data channels 1 clock channel	2.5Gbps (RX/TX) 4 data channels 1 clock channel	2.5Gbps (RX/TX) 8 data channels 2clock channel	2.5Gbps (RX/TX) 8 data channels 2clock channel	2.5Gbps (RX/TX) 8 data channels 2clock channel
MIPI C-PHY Hard Core	TBD	0	2.5Gbps, (=5.75Gbps, RX/TX), 3 dat channels	0	0
CPU Core	0	S=Cortex-M4	0	0	S=RiscV AE350_SOC
ADC	1	1	1	2	2
GPIO Bank	4	8	11	6	6
Maximum number of I/O	69	236	320	376	376
Core Voltage	0.9V/1.0V/1.2V	0.9V/1.0V/1.2V	0.9V/1.0V	0.9V/1.0V	0.9V/1.0V

Free IP Licensing	
PCIE 2.0	Rapidio
SGMII	SDI-Tx/Rx
1000 Base-X	eDP-Tx/Rx
10G Base-R	DP-Tx/Rx
XMAC	SLVS-EC-RX
XAUI	HDMI
CPRI	USB3.1
JESD204B	ISP



SERDES Eye Diagram



2.5 Gbps



5Gbps

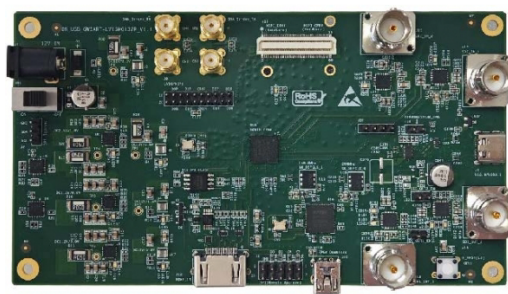


10Gbps

Development Kits



DK_START_GW5AT-LV60PG484A_V1.1



DK_USB_GW5ART-LV15MG132P_V1.1

